IN THE SPECIFICATION:

On page 1, before line 1, please insert the following new paragraph:

--**CROSS-REFERENCE TO RELATED PATENT APPLICATIONS**

This Patent Application is a Divisional Patent Application of and claims, under 35 U.S.C. §120, the benefit of U.S. Patent Application Serial No. 10/165,264, filed on June 6, 2002.--

Please replace the paragraph starting on page 1, line 16 with the following amended paragraph:

Semiconductor memory chips, such as dynamic random access memory (DRAM), typically include array regions, including arrays of memory cells, as well as support regions, which include logic devices that provide support functionality. As dimensions shrink to 110 nm and below, DRAM technologies face several critical challenges. The cell design must be "friendly" for lithography and ~~all~~ for the use of self-alignment techniques in the array. For example, misalignment of interconnection and contact structures can result in problems such as leakage or shorts, and increased resistance, affecting both functionality and performance.

Please replace the paragraph starting on page 2, line 2 with the following amended paragraph:

Conventional methods of forming contacts and interconnection structures involve multiple processing steps, including lithographic masks for contacts and interconnection features at the minimum lithographic dimensions (i.e. minimum feature size). Processes involving masks having minimum feature sizes are relatively costly, and the ~~difficultly~~ difficulty of achieving overlay of such features without misalignment between different processing levels increases.

Please replace the paragraph starting on page 2, line 10 with the following amended paragraph:

An example of a conventional wiring and contact layout in an array region is illustrated in the plan view shown in FIG. 8A, where source/drain diffusion regions (active areas AA) 110 on a substrate ~~is~~ are oriented along ~~a~~ vertical lines, and word lines 130 are formed over the substrate, running horizontally across the diffusion regions 110. Wiring lines 120 (such as bit lines) might be laid out to run parallel and overlaying the diffusion regions 110. Although it is preferable for the wiring lines 120 to be aligned over the diffusion regions 110, typically there will be some misalignment, as illustrated in FIG. 8A. Note that the illustrations are not intended to be drawn to scale, and the misalignments shown are exaggerated for illustration purposes. Contact via holes 150 may be laid out to define contact structures for connecting the wiring to diffusion regions of devices (not shown) that are formed in the substrate.

Please replace the paragraph starting on page 3, line 19 with the following amended paragraph:

Divakaruni et al. (U.S. Patent No. 6,245,651) proposed a method for creating self-aligned borderless contacts in which a first dielectric layer is formed in both the array and support regions, and then an etch stop layer is formed over the support region. The array regions include gate stacks in the first dielectric layer, and diffusion regions between the gate stacks in the substrate, to which bitline contacts are to be formed. A second dielectric layer is then deposited over the array region and the support region, which includes the etch stop layer in the support region. The second dielectric layer is patterned to define the interconnect structures. Etching of the second dielectric layer is performed to form the interconnect structures in both the array and support regions. The etch stop layer in between the first and second dielectric layers stops the etching in the support region, but allows further etching in the array region to form the contacts, which are borderless to the gate stacks and provide contact to the diffusion regions. Subsequently, the contacts and interconnect structures may be filled with a conductive material, for example, using a damascene process. However, the method of Divakaruni et al. has the disadvantage that the buried etch stop layer in the support region produces topographical anomolies that makes removal of excess conductive material difficult in the planarization step of the damascene process. In addition, the use of separate dielectric and etch stop layers in the method of Divakaruni et al. adds complexity to the processing, and tends to increase costs.

Please replace the paragraph starting on page 9, line 3 with the following amended paragraph:

Referring to FIG. 1A, a plan view of a layout in a memory array region (for example, a DRAM memory array) on a substrate of a semiconductor chip. Source/drain regions 110 in the substrate (which are typically doped regions, also known as active area, or AA regions 110) are laid out in this embodiment in a linear fashion, for example, by using a line-type mask. Memory cells (not shown) are formed along the AA regions 110 at or near the intersection of the AA regions 110 and the word lines 130. Note that in some embodiments, the word lines 130 may function as gate conductors at the intersection with the diffusion regions 110. Thus, in accordance with the present invention, gates stacks 130 that are encapsulated in a dielectric 115, for example, as illustrated in FIG. 2B, are associated with the source/drain diffusion regions 110, and referred to hereinafter interchangeably with word lines 130. The word lines 130 may be laid out essentially orthogonally to the orientation of the diffusion regions 110, but could also be laid out to cross the AA patterns 110 (which are lines in this example, but could take arbitrary paths in other embodiments) at other angles. Isolation regions 140 are formed in the substrate between the diffusion regions 110. Wiring lines (such as bitlines) 120 are typically formed over the devices formed in and on the substrate. The wiring lines 120 are preferably laid out to be aligned with the diffusion regions 110, but typically there is some overlay misalignment between the wiring lines 120 and the AA or diffusion lines 110, as illustrated in FIG. 1A. The present invention provides a method for forming contacts between the wiring lines 120 and the diffusion lines 110 that are self-aligned to the wiring lines 120 which minimizes problems caused by misalignment

of contacts and reduces processing costs compared to prior methods.

Please replace the paragraph starting on page 10, line 1 with the following amended paragraph:

In accordance with the present invention, a substrate 10 is provided at an intermediate stage in which devices may be formed in both an array region 910 and a support region 920. FIG. 2A shows a cross-sectional view along the direction of line B-B' of ~~FIG. 1~~ FIGs. 1A and 1B extending through the array region 910 and support region 920. In the array region 910, doped portions of the substrate 10 form the diffusion regions 110. Isolation trenches 140 containing a dielectric material such as silicon oxide have been formed. A support device 230 is formed in the support region 920 having support device diffusion regions 111. Array devices (not shown), are formed in the array region having diffusion regions 110. The array devices, such as memory cells, are required to be densely packed. The memory cells may include planar or trench-type (vertical) devices. Word lines 130 are formed in a layout that intersects the layout of the diffusion regions 110, as shown in the cross-section in FIG. 2B along the line A-A' of FIG. 1A. The word lines 130 may be formed within a dielectric material 115, as illustrated in FIG. 2B, such as silicon nitride, which provides protection from shorts which may occur during the contact etch. In order to integrate the array devices into a circuit, contacts must be formed between the array device diffusion regions 110 and circuit wiring. FIG. 2C illustrates a cross-section of the structure of FIG. 1A or 1B

along the line B-B', wherein isolation trenches 140 separate diffusion regions 110. Corresponding cross-sections along the line A-A' are illustrated in FIGs. 3B, 4B, 5B, 6B and 7B, and along the line B-B' in FIGs. 3C, 4C, 5C, 6C and 7C, as described in more detail below.

Please replace the paragraph starting on page 13, line 17 with the following amended paragraph:

Subsequently, the mask 540 is removed. The wiring and contact openings may now be filled with conductive material 620, 740 using processes known in the art, resulting in the structure illustrated in FIG. 7A. For example, barrier layers (not shown) are typically formed in such openings to protect against undesirable interactions between the conductive material and adjacent materials. The conductive materials in the contact structure 620 and interconnect or wiring structure 740 could be the same or different conductive materials, depending on the application, but are shown separately here to illustrate that the contact structures 620 and the wiring (interconnect) structures 740 formed in accordance with the present invention are self-aligned. Conductive materials for the contact structures 620 could include, for example, tungsten, polysilicon, polysilicide or even stacked conductor combinations. Conductive materials for interconnect structures 740 may include tungsten, aluminum, or possibly copper. The hardmask layer 220 will be removed during this process, for example by planarization methods such as chemical-mechanical polishing (CMP) or an etchback method. Cross-sections of the resulting structure along lines A-A' and B-B' are illustrated in FIGs. 7B and 7C, respectively.